A Fully Integrated Variable Gain 5.75-GHz LNA with on chip Active Balun for WLAN

M.Kumarasamy Raja, Terry Tear Chin Boon, K.Nuntha Kumar and Wong Sheng Jau

Institute of MicroElectronics (IME), 11, Science Park Road, Singapore- 117685

Abstract — **A 5.75-GHz variable gain Low Noise Amplifier (LNA) using 0.18 μm CMOS process is described. A novel gain control technique is proposed which does not affect the matching at the input and output and the gain flatness of the LNA when the gain is varied. Usage of Gain control to achieve low noise figure and high IIP3 simultaneously without increasing the power consumption is demonstrated. Another feature of this LNA is that it also acts as an active balun for converting the single-ended input to a differential output. The LNA does not need any off-chip components and is matched to 50-Ohm. Measured results of this LNA in commercial SOC-16 package include a gain of 21 dB, noise figure of 4.4 dB, gain variation of 10.5 dB and an IIP3 of −6.5 dBm . It draws 9 mA from 1.8 V power supply. The chip area excluding the pads is 0.5mm×0.6mm.**

I. Introduction

Development of transceiver chips in the 5.25-GHz and 5.8-GHz band has picked up momentum in last couple of years following the IEEE standards WLAN 802.11a. LNA is an important block of the receiver since its NF and gain contribute significantly to the overall Signal to Noise Ratio (SNR) of the receiver. Design of LNA involves trade-off between NF, matching, stability, gain, IIP3 etc. In addition, the parastics due to package and interconnects need to be considered carefully. Introducing gain control at the LNA not only reduces the current consumption of LNA for given linearity, but also helps to reduce the current consumption of the following blocks owing to reduced linearity requirements.

Differential architectures are preferred in CMOS technologies since they are less susceptible to common mode noise. Conventional CMOS receiver architectures use an off-chip balun in front of the cascode differential LNA [3]. The disadvantage of this scheme is that the overall receiver NF is degraded by the insertion loss of the balun. Also the cost of the receiver goes up due to the off-chip balun. The second stage of the proposed LNA uses the concept of active balun to convert the single-ended (unbalanced) RF signal to a differential (balanced) signal, in addition to providing gain. Hence the receiver using proposed LNA not only offers a better overall NF, but also proves to be cost-effective.

II. Gain Control

The NF of LNA is dictated by the sensitivity specification (the lowest power to be received at the specified BER) of the receiver to cater for the weakest received signal. The LNA offers the highest gain and lowest NF in its High Gain mode for the weak signal. But under strong received signal conditions the LNA and the whole receiver gets saturated and hence the linearity (IIP3) specification also needs to be met. To satisfy the linearity requirement the proposed LNA operates in the Low Gain mode under strong signal conditions. It may be noted that a slight degradation in NF is of no harm when the received signal strength is high as the demodulator in the receiver chain can operate satisfactorily as long as the SNR at its input is above a threshold value. The LNA meets a better IIP3 performance in Low Gain mode and puts a relaxed IIP3 requirement on the following blocks. Gain reduction in LNA also reduces the dynamic range of the Automatic Gain Control (AGC) circuitry, which is implemented in the IF after the down-conversion mixer. Usually with the reduced dynamic range, the SNR performance of the AGC is improved.

One of the popular method of controlling the gain of the cascode LNA is by diverting a portion of drain current from the cascode transistor through another MOSFET [3]. This scheme of gain control significantly degrades the NF and IIP3 in the Low Gain mode. An enhanced scheme proposed in [4] controls the gate bias of the PMOS transistor in the folded cascode topology and does not sacrifice the NF in Low Gain mode. The gain control scheme proposed here not only achieves a better NF but also a superior IIP3 in the Low Gain mode. The gain control circuitry also is simple and does not put any restriction in the other portions of the circuit. Input and output ports are well isolated from the gain control circuit so that the matching at these ports is not affected during gain variation. The gain flatness is also observed to be better when the gain is reduced.

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III. THE TWO STAGE VARIABLE GAIN LNA

The circuit diagram of the proposed LNA is shown in Figure 1. It consists of two stages and the gain control circuit. There is a single RF input RFin and two differential outputs RFout1 and RFout2. The LNA operates from a supply voltage of 1.8 V and draws a total current of 9 mA. In a two stage LNA, the first stage has to be optimized for NF and the second stage needs to be optimized for IIP3 [6]. While the NF of the first stage depends on *gm* of the transistor, the IIP3 depends on the gate overdrive voltage, both of which depend on the bias current I_D and width of the MOSFETs. Hence, the design of the two stages involves selection of optimum width and drain current I_D.

A. First Stage

The first stage of the LNA is the cascode circuit employing inductors at source and gate of the input transistor M1 for input matching at the desired frequency and a load inductor at the output transistor M2 to get the output matching as shown. The design of this stage is well explained in [1] and [2]. The gate inductance of M1 is realized by the bondwire due to two reasons. One reason is that the bondwire usually offers a better Q than the on chip inductors and hence is preferred to achieve a better NF performance. Secondly the LNA or the transceiver containing the LNA needs to be packaged ultimately for commercialization and hence the effect of bondwire at the RF input port needs to be accounted for.

Width of transistor M1 is selected such that it offers the least NFmin at the desired operating frequency and desired drain current. For a power constrained design, the optimum width is given by [1]

$$W_{opt\,P} \approx \frac{1}{3\omega L C_{ox} R_s} \tag{1}$$

In (1) ω is the operating frequency, L is the length of MOSFET (0.18 microns in our case), C_{ox} is the capacitance per unit area of the gate oxide. The series combination of gate inductance L_g and the source inductance L_s of M1 resonates with C_{gs} of M1 at the operating frequency as below

$$\omega = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{2}$$

Under this condition the input impedance R_s (usually is 50 Ohm) is purely resistive and is given by

$$R_s = 2\pi f_T L_s \tag{3}$$

(2) and (3) form the design equations for L_g and L_s.

B. Gain Control Circuit +

The transistor M3 in series with the inductor L_X is connected between the output node of the first stage P to ground as shown. The gate bias voltage is the gain control voltage Vc and is varied from 0 to Vdd (1.8V). When Vc=0V, M3 is OFF and the gain control circuitry offers high impedance at P with respect to ground. Hence, output of the first stage is delivered to the second stage and the whole LNA operates in High Gain mode. When Vc=Vdd (1.8V), M3 will be in ON state and offers a low resistance between its drain and source. Now, L_X appears effectively across the load inductance of the first stage, thereby reducing the overall load inductance and hence results in reduced gain of the first stage. In other words, part of the output of first stage is shunted to ground and hence the overall gain is reduced. The advantage of this scheme over [3] is that the drain current of M1 and M2 (and hence the gate over drive) remains the same, even in the Low Gain mode and hence the NF and IIP3 performance of the first stage is not sacrificed.

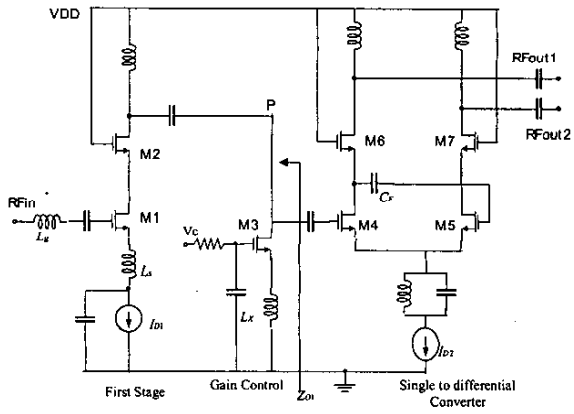

Fig. 1. The circuit diagram of the variable gain LNA.

In order to maintain the gain flatness, the second stage must see an inductive impedance at point P (Z_{01}) with respect to ground in the desired frequency band. When M3 is ON, this condition is met due to the presence of inductor L_X. In the absence of L_X, Z_{01} would have been capacitive due to the presence of C_{gs} and C_{sb} of M3. When M3 is in OFF State Z_{01} is inductive due to the load inductance of the first stage. When Vc takes on values between 0 and 1.8V, M3 acts as a voltage

+ Patent pending

controlled resistor. Size of M3 determines the amount of gain control that can be achieved. The resistor and the capacitor in the gate of M3 isolate the RF signal from the control voltage Vc.

C. Second Stage

The second stage is differential cascode structure as shown in Fig. 1. Drain of M4 is connected to the gate of M5 through C_F to support the single to differential conversion [5]. The parallel tank circuit at the sources of the differential pair M4 and M5 is designed to resonate at the operating frequency. It offers high impedance at the operating frequency (5.75 GHz) thereby improving the virtual ground. Besides this, it isolates the common mode noise from interfering the circuit operation. The load inductors and capacitors decide the output matching.

IV. LAYOUT AND PAD CONSIDERATIONS

The LNA was implemented using standard 0.18-μm RFCMOS technology and was packaged in SOC-16 package. The chip micrograph is shown in Figure 2. The chip includes the current mirror and all the biasing circuits, which were not shown in Figure 1 for clarity.

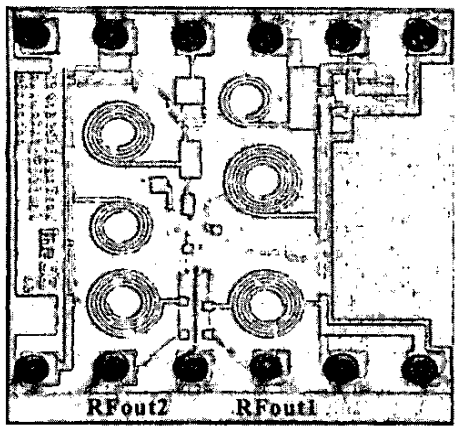

Fig. 2. The chip micrograph of the variable gain LNA

The RF input (RFin) is at the top and the RF output terminals (RFout1 and RFout2) are in the bottom. The signal is routed in such a manner that it is unidirectional from top to bottom. The pad size used is 70 microns. Smaller pad size means a lower parasitic capacitance to ground and hence a lesser degradation in NF. One of the ground pads was down bonded to the package ground to reduce ground inductance. For the same purpose two VDD pads were used. All the inductors are spaced sufficiently away from other components to avoid magnetic field coupling. Substrate contacts were made around the chip and connected to ground to improve grounding. Care was taken to make the layout of second stage symmetric.

V. MEASURED RESULTS

The chip was packaged on a commercial SOC-16 package and tested in BT resin PCB. The measured results are summarized in Table I. The NF and gain when Vc=0 and Vc= 1.8V are shown in Figures 3 and 4 respectively. The gain vs Vc is shown in Figure 5.

TABLE I
SUMMARY OF MEASURED RESULTS

Parameter	Measured Value	
	High Gain	Low Gain
Frequency [GHz]	5.65-5.85	5.65-5.85
Gain (|S21|) [dB]	21.4	10.8
Noise Figure NF [dB]	4.4	6.2
IIP3 (dBm)	-18.5	-6.5
|S11| [dB]	Better than 7	
Drain Current (mA)	9 from 1.8V supply	

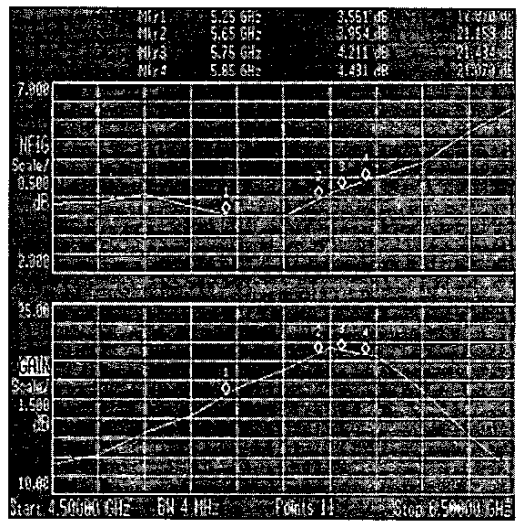

Fig. 3. Gain and NF vs. Frequency (High Gain Mode)

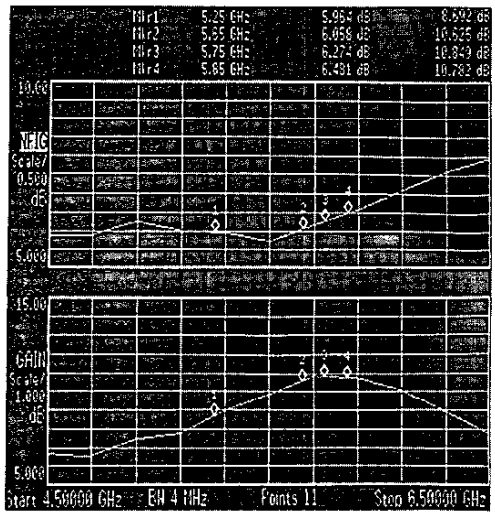

Fig. 4. Gain and NF vs. Frequency (Low Gain Mode)

The two-tone IIP3 performance of the LNA was tested by feeding two signals whose frequency differs by 100 kHz. It may be noted that the improvement in IIP3 is 12 dB (from High gain mode to the Low gain mode) which is about 1.5 dB better than the gain reduction . Also the NF degrades only by about 1.8 dB in the Low gain mode. Lower NF even in Low Gain mode offers freedom in the receiver design as some amount of linearity can be traded off for the NF when the demodulator performance depends on its input SINAD (Signal to Noise+Distortion ratio) rather than SNR.

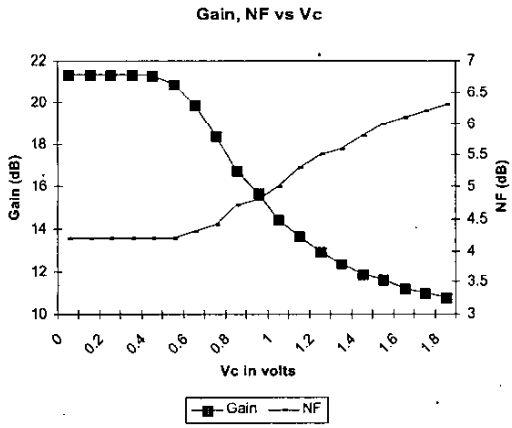

Fig. 4. Gain And NF Vs. Vc

VI. Conclusion

A two-stage variable gain LNA operating at 5.75 GHz using standard 0.18-micron CMOS technology in SOC-16 package was demonstrated. The LNA was observed to give an improved NF and IIP3 even in the Low Gain mode since the gain control circuitry is totally passive. The second stage also serves as an active balun. While the usage of gain control reduces the IIP3 (and thereby the power consumption) requirements, the active balun helps to avoid the offchip balun which can degrade the overall NF.

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